A DATA COLLECTION SYSTEM FOR THE SDC STRAW TUBE TRACKER

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INTRODUCTION

The Solenoid Detector Collaboration (SDC) has proposed to construct and operate a large, general-purpose, solenoidal detector that combines excellent charged particle detection, a hermetic, scintillator-based calorimeter and a large muon identification system.[1] A principle component of the SDC detector is the outer tracker that provides precise momentum measurement of charged particles from a radius of 85 cm to 165 cm from the proton beam. The outer tracker front-end electronics capture and digitize the data it produces and a data collection circuit (DCC) collects this data and passes it to the SDC data acquisition (DAQ) system. We describe in this article the specifications and design of the outer tracker DCC.

OUTER TRACKER DATA COLLECTION CIRCUIT

The outer tracker consists of 137,000 straw tube chambers that provide timing information used to measure the position of charged particles. The analog signals are processed using an amplifier-shaper-discriminator circuit[2] and are digitized by a time memory chip[3] (TMC). The digitized data is held by the TMC and a level 2 buffer (L2B) until a decision to either reject or accept the data is made by the level 1 and level 2 (L2) trigger system. Upon a L2 trigger accept signal, the DCC acquires the relevant data from the TMC/L2B's, formats it into data packets, and passes these packets to the DAQ system. Each TMC/L2B instruments four straw tubes, eight TMC/L2B s are arranged on a small PC board (Time Memory Assembly or TMA), and either five or seven of these boards are mounted in a small housing known as a

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Figure 1. The data collection circuit described in the text. Each FMUX reads out eight TMC/L2B chips, and either five or seven FMUX's are connected together and read out 156 or 212 straw tubes, respectively. The CIC is located in an SDC standard DAQ crate.

microcrate. Each microcrate instruments the 212 (156) straws of an axial (stereo) module of the outer tracker.

Our proposed DCC system[4] consists of two levels: i) an application-specific integrated circuit known as the Front-End Multiplexor (FMUX) located on each TMA, and ii) a set of high-performance, low-cost microprocessors (Crate Interface Processors or CIP's) that collect the data from the microcrates. Each FMUX collects data from eight TMC/L2B chips for a given interaction. Once all the data has been collected, the FMUX transmits this data to a CIP located on a Crate Interface Card (CIC) that reside off the detector. Each CIC has four CIP's that process the data from eight microcrates. A total of 96 CIC cards are required to collect the data for the outer tracker. The CIC cards are housed in SDC Standard DAQ crates, each of which are expected to carry 12 CIC's. The CIC format and compress the data for each interaction and then transfer the data to the DAQ system via a Scheduler/Monitor Processor (SMP). We illustrate this system in Fig. 1.

DCC Design Specifications

We have performed detailed Verilog[5] simulation studies in order to estimate the DCC buffering and bandwidth requirements.[4] Although other studies have been made of data collection and DAQ systems for SSC detectors,[6] they have either been generic in nature or focused on devices that present different data collection issues (such as the SDC calorimeter). We took into account the physics correlation of data, multiple interactions in the same beam crossing and crossings adjacent in time to the trigger, and the effects of finite buffer sizes and bandwidths. These studies show that the occupancy of a single straw tube could be as large as 0.10 hits/interaction at the design SSC luminosity of 10^{33} cm^{-2}s^{-1}. The DCC will therefore read out an maximum average of 0.4 hits/event from each TMC/L2B. The rate of interactions accepted for read out (the L2 rate) are expected to be of order 10^3 Hz, but we have conservatively assumed a maximum rate of 10^4 Hz. We estimate that it will require 3 bytes to encode each datum, so an average maximum bandwidth of $\sim$ 10 Kbytes/second between each TMC/L2B and FMUX is required. Our simulation studies have shown that a maximum burst bandwidth of $\sim$ 100 Kbytes/second is sufficient.

The DCC will read out anywhere from zero to $\sim$ 10 data from each TMC/L2B for a specific interaction. A data-driven DCC is therefore attractive as it minimizes the amount of buffer space and bandwidth, and it decentralizes the control of the system. However, it is not possible to anticipate the total amount of buffer space required at each stage in the system, so conservative estimates must be made of the necessary buffer space in order for the system to function with high data collection efficiency. In any event, the system must be able to recover gracefully when one or more buffers fill completely.

The preliminary specifications for the SDC DAQ system require that data be collected in channel and event order. Channel ordering of the data can be ensured by reading out the TMC/L2B's in order after the data for an interaction is available. This would require the DCC to begin data collection only when the data for the first channels are available. It implies that data for a subsequent trigger must be held until all of the TMC/L2B chips have been read out for the current trigger. However, we assume that data can be passed to the DAQ system regardless of event order as long as the data packets contain the information necessary to identify the interaction the data is associated with.

The DCC must be highly reliable, as many of its components will be installed in areas that will be infrequently serviced. The system must also be fault-tolerant, so that a single component failure does not significantly impact the overall performance of the system.

Features of Proposed DCC

Our proposed DCC operates in a data-driven mode where data is read out of each TMC/L2B whenever it is available by the FMUX and stored in a FIFO buffer. The first FMUX in a microcrate waits until all eight of its TMC/L2B chips have signalled the data for the next trigger has been transferred to the FMUX buffers. The FMUX then transmits the data from its buffer to the CIC and signals the next FMUX in the microcrate. This continues until the entire microcrate is read out. The CIC formats the data from each microcrate as it appears in an input buffer. When all data has been collected from the microcrates serviced by a CIC card, the CIC transfers the data packet to the DAQ system. Our studies have shown this system to be able to handle the dataflow requirements of the outer tracker.

The interface between each TMC/L2B and FMUX consists of 2 control lines and 4 data signals. The relatively modest bandwidth requirement allows us to clock the data into the FMUX at a rate of $\sim$ 2 MHz, which reduces the digital noise that could affect the performance of the nearby analogue electronics. Three redundant, bit-serial lines are used to transfer the data from the FMUX to the CIC using a group encoding scheme that is robust and self-synchronizing.

Most of the monitoring functions in the DCC are implemented in the CIC. We have determined that currently-available microprocessors are sufficiently powerful to be able to validate each datum as the CIP creates the data packets. This allows the CIP to check for data integrity and to log any exceptions encountered. The CIP can also keep statistical information such as the amount of data read out and the number of exceptional conditions encountered, and provide that information upon request.

We expect the reliability of the DCC components to be high given the level of integration used in the custom digital circuits and the use of commercial components for the CIC. We therefore believe the largest potential source of failure will be interconnections between components. Our DCC design reduces the exposure to such failures in two ways. A failure of a single TMC/L2B will only affect the four channels readout by that chip and not compromise the readout of the 7 other TMC/L2B's on the same TMA (this is not necessarily true if all TMC/L2B's were read out using a single bus. Data transmission from the FMUX's can take place over any one of the three bit-serial data paths connected to the microcrate (the datapath in use is configurable). This reduces the impact of a failure in a specific FMUX; only data from the 32 channels read out by that FMUX would be compromised.

We are continuing a more detailed fault analysis in order to pinpoint other aspects of the design that could cause significant loss of system capability.

Prototype Development and Conclusions

We are currently engaged in an R & D program to build a DCC prototype system. A prototype FMUX with virutally all of the functionality described above is currently being manufactured by Northern Telecom. This prototype will be able to read out two TMC/L2B's and has a buffer depth of 8 hits for each TMC/L2B. This design will subsequently be scaled up for eight TMC/L2B chips and a 16-deep data buffer.

We have developed a conceptual design for the CIC and expect to have a detailed layout of a prototype board completed by fall 1993. This prototype will be implemented on a 6U standard VME card and will be designed to readout a single set of FMUX's.

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