This is a circuit diagram for the FINDER interface circuit. VME represents the user, and the other blocks represent the six different modules of the circuit. The modules ADDRESS BUFFER, CLOCK GEN, CONTROL, FIFO, and READOUT are being designed for this project.

This is a block of Verilog code that defines the FIFO module. This identifies the inputs and outputs of the FIFO module, the relationships between the different wires in the module and the logical conditions that the circuit will react to.

These diagrams represent the patterns that the FINDER looks for. On the left is a diagram of all of the energy patterns observed during one matter-antimatter collision (these are shown in yellow). On the right is a diagram of the tracks found by the FINDER chip (these patterns are shown in blue). As you can see, the FINDER chip takes in all of the information gathered during the experiment and sorts through it in order to find the pertinant information.