Status of XFT Development

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1. FINDER status
   - Functionality
   - Methodology
   - Status of Testing
2. LINKER progress
3. Schedule

CDF/IPP Meeting
December 9, 1994

XFT Trigger for CDF

XFT is a replacement for the CFT trigger

- Will operate at L1
- Find tracks every 132 ns
- Momentum resolution $< 0.02p_T$
- Fake rate rejection $\times 2$ better than CFT

Project responsibilities

- Rochester
  - simulation and design
  - debugging
- Fermilab
  - XFT PC Boards, crates
  - TDC auxiliary cards
  - design and simulation
- IPP
  - Design and fabrication of ASIC's
    1. FINDER
    2. LINKER

$\boxed{\text{FINDER Functionality}}$

FINDER functionality defined in draft XFT Design Report and internal documentation:

1. Find patterns in interactions separated by 132 ns

2. Selectable between SL 2,4,6 and 8

3. Number of misses allowed between 0 and 3

4. 4 storage buffers for timing data
   - "core" 12 wires for L1 accepts
   - buffers selectable at time of L1 accept
   - readout via two independent buses

5. L1 delay variable
   - Minimum delay 31×64 ns $= 1.984\ \mu$s
   - Maximum delay 95×64 ns $= 6.080\ \mu$s

6. Handle "dead" wires (set them on)

7. JTAG for configuration (MS, SL, L1delay, dead wires)

8. JTAG for scan paths (6 independent loops)

9. Master reset to bring FINDER to default configuration

Testing Methodology

Know correct FINDER behaviour from XFT simulation

- Patterns used in FORTRAN code $\Rightarrow$ generate Verilog
- Test Verilog definition of FINDER using these patterns
- Run design in 1 ns timing steps
- Verify that all output is correct
  - Phi pixel output
  - d1 and d2 databus output under various conditions

LSI Logic synthesizes Verilog code to gate level/layout

- Provide anotated verilog code with gate and wire delays
- Repeat same tests
- Test for timing robustness

Sign-off for production

- Fabricate chip
- Test for functionality and yield on tester using our test vectors (32K)

Summary of Test

Test on a large set of patterns

- Use both "I/O control pins" and JTAG for configuration
- Approximately 200 patterns for each superlayer
  - 3 different choices of miss count (0, 2, 3)
  - will use 10K test vectors
- Verify readout of d1 and d2
  - overlapping L1 triggers
  - multiple use of same buffer
  - multiple readout of d1 and d2

Verify functionality of JTAG

- Define set of test vectors that exercise all features
  - Will be of order 5K test vectors
  - Verify that configuration control works
  - Verify all scan paths are functional
  - Reset behaves correctly

Remaining test vectors for additional yield tests

Status of FINDER Validation

Have tested all Superlayer patterns

- Tested all Superlayers with MS=2
- Exhaustive tests with MS=0, 1 and 3 not yet completed
- Still need to check out-of-time performance

Have verified JTAG functionality

- Have sets of test vectors
- Still need to amalgamate into one complete set

Additional yeild tests not defined yet

- Will happen when LSI provides timing data

Schedule for FINDER

Have had stable Verilog code since November 4

- Have incorporated LSI's enhancements to Verilog
- Are still concerned about some timing issues
- Expect annotated Verilog design next week

Will take of order 1 week to define tests for yield

- Will submit for fabrication mid-December
- parts returned mid to late January

LINKER Status

Have completed 0th-version of LINKER Verilog design

- incorporated all “tricks” from FINDER experience
  - No internal tri-state buses
  - Avoid use of “initial” statement
  - Avoid certain types of Verilog constructs
  - Clock distribution designed robustly
- LSI personnel also up-to-speed

Focus will turn to LINKER testing in early January

- Have started looking at test patterns
- Design to settle by February 1, 1995
- Submitted for fabrication by March 1, 1995
- Components returned by April 1, 1995

Future IPP Involvement

The ASIC development will require us to

- set up a small test stand to evaluate ASIC's
- verify functionality
- develop control software

Future tasks

- develope on-line software to control and diagnose system
- integrate XFT into detector (summer 1995)
- measure real-time performance